FIG. 1

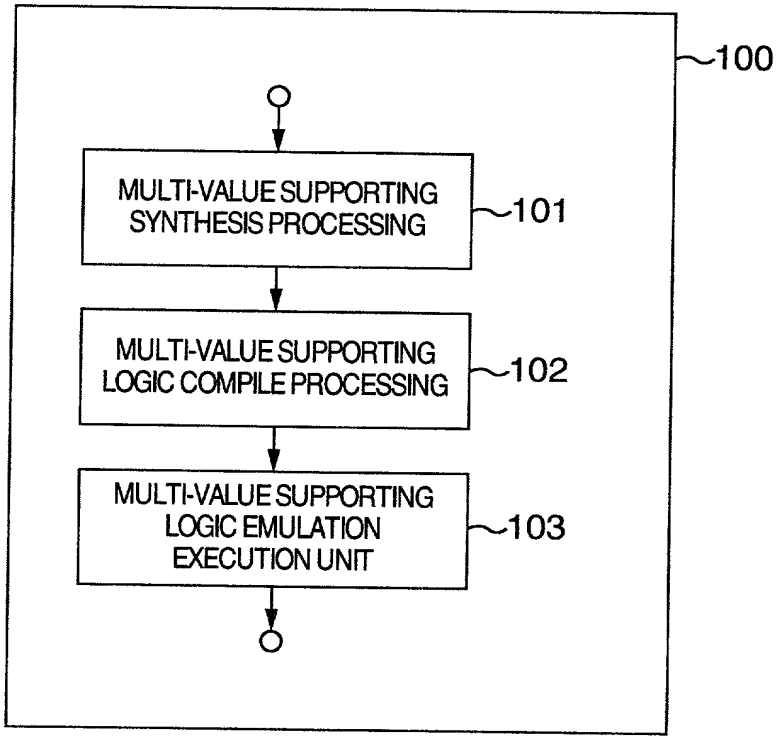

100
MULTI-VALUE SUPPORTING SYNTHESIS PROCESSING
101
MULTI-VALUE SUPPORTING LOGIC COMPILE PROCESSING
102
MULTI-VALUE SUPPORTING LOGIC EMULATION EXECUTION UNIT
103

FIG. 2

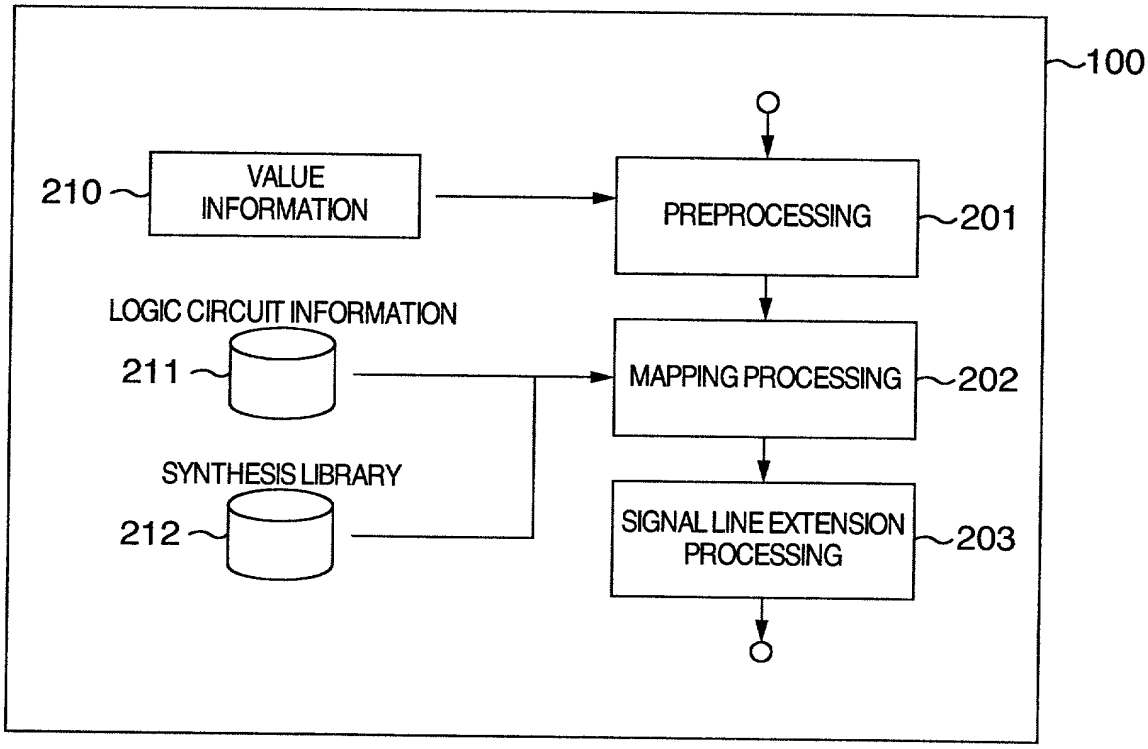

100
210
VALUE INFORMATION
PREPROCESSING
201
LOGIC CIRCUIT INFORMATION
211
MAPPING PROCESSING
202
SYNTHESIS LIBRARY
212
SIGNAL LINE EXTENSION PROCESSING
203

FIG. 3

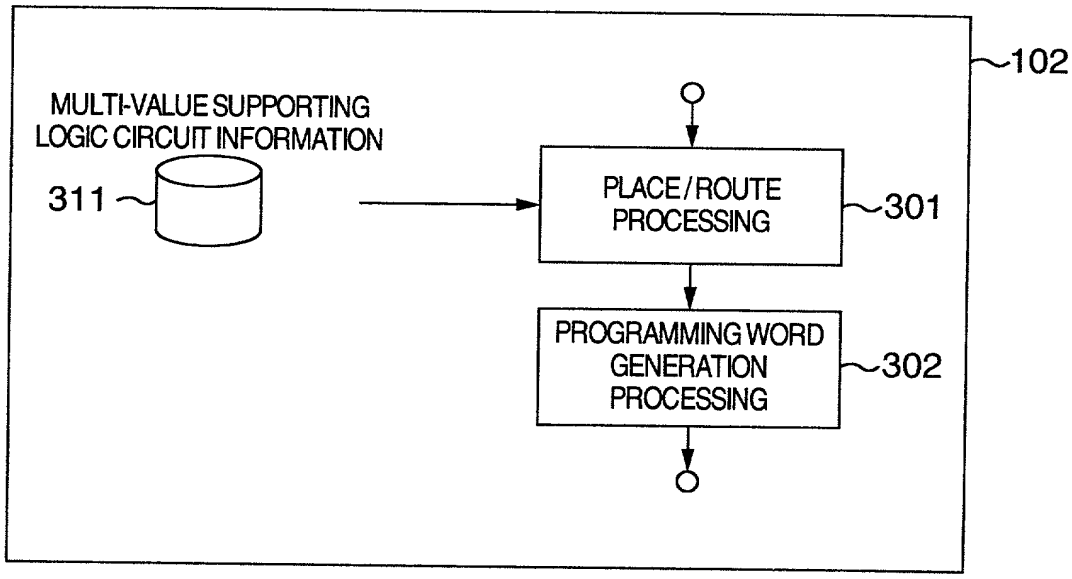

102
MULTI-VALUE SUPPORTING LOGIC CIRCUIT INFORMATION
311
PLACE/ROUTE PROCESSING
301
PROGRAMMING WORD GENERATION PROCESSING
302

FIG. 4

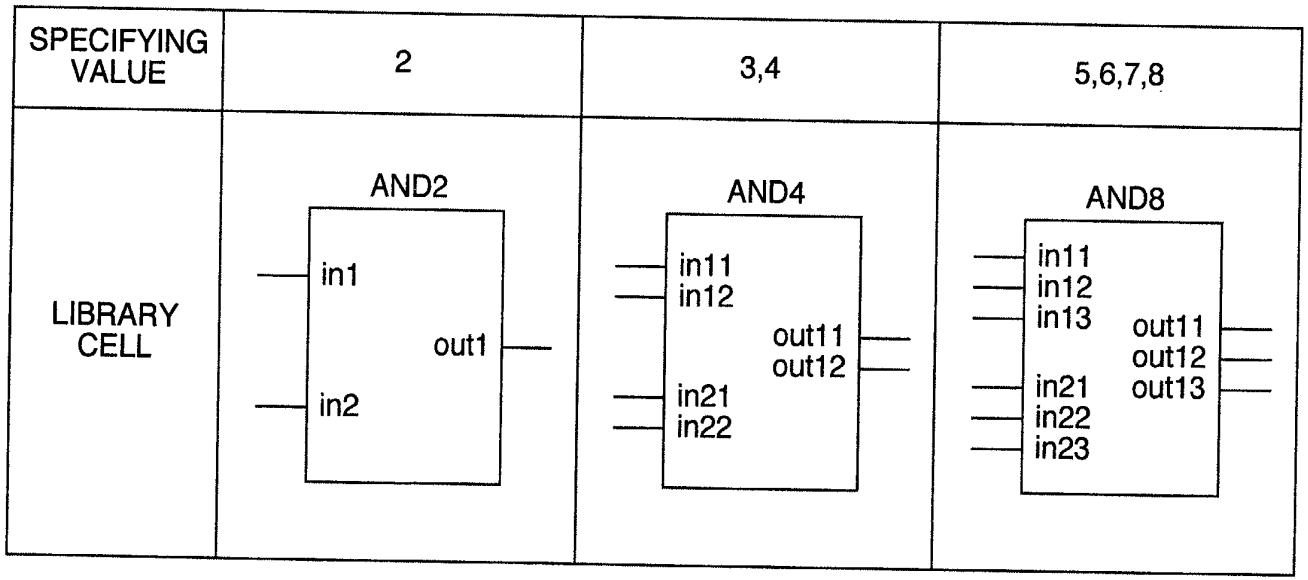


FIG. 5

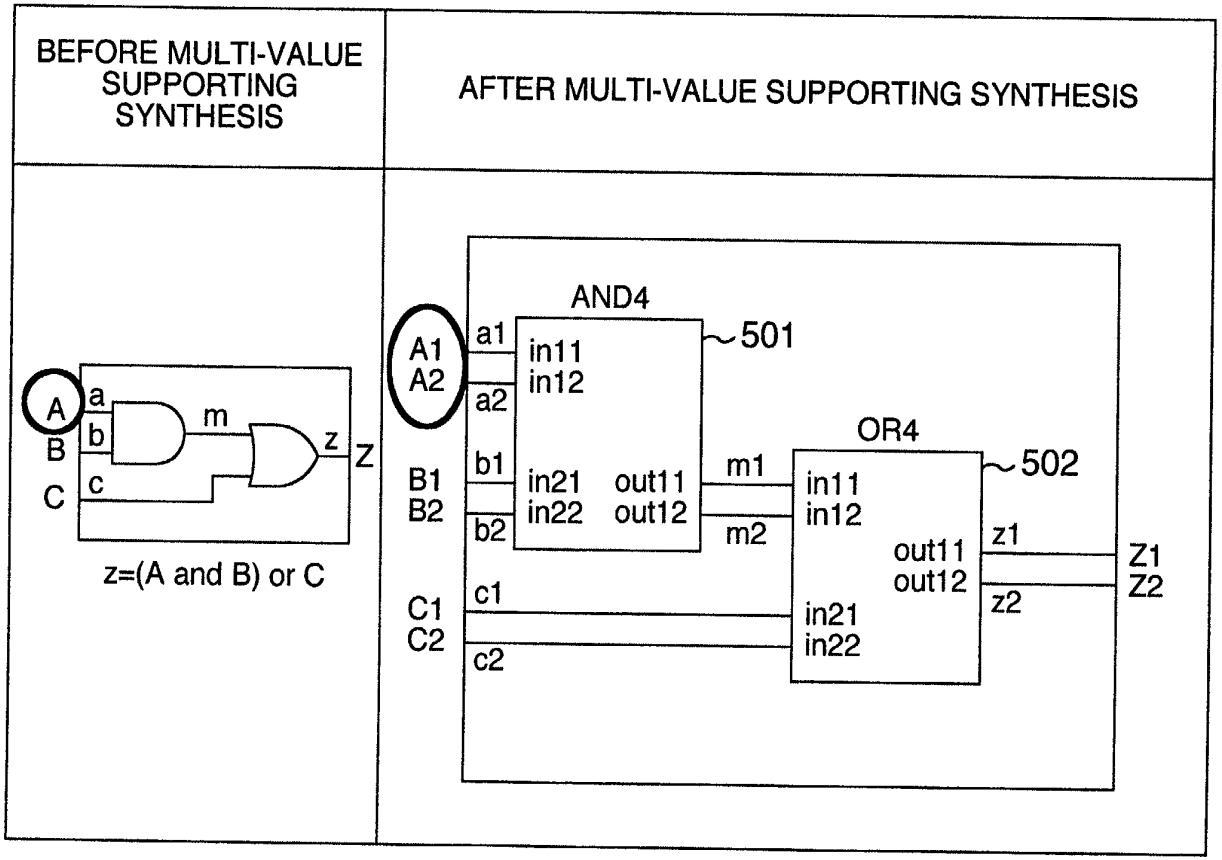


FIG. 6

600

601 LOGIC SIGNAL	602 PHYSICAL SIGNAL	603 TYPE	604 ATTRIBUTE
A	A1,A2	PORT	IN
B	B1,B2	PORT	IN
C	C1,C2	PORT	IN
Z	Z1,Z2	PORT	OUT
a	a1,a2	INTERNAL	———
b	b1,b2	INTERNAL	———
c	c1,c2	INTERNAL	———
z	z1,z2	INTERNAL	———
m	m1,m2	INTERNAL	———

FIG. 7

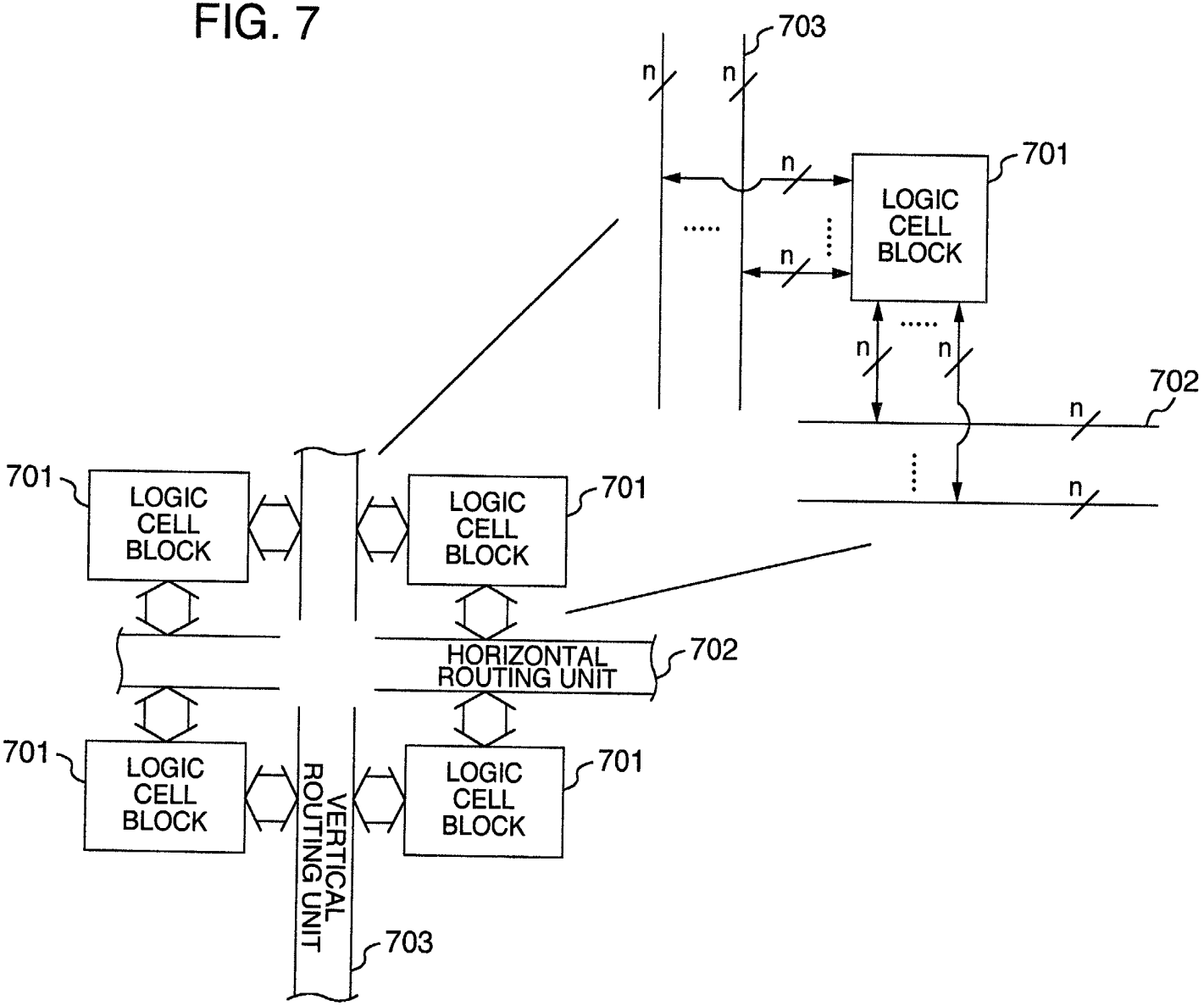


FIG. 8

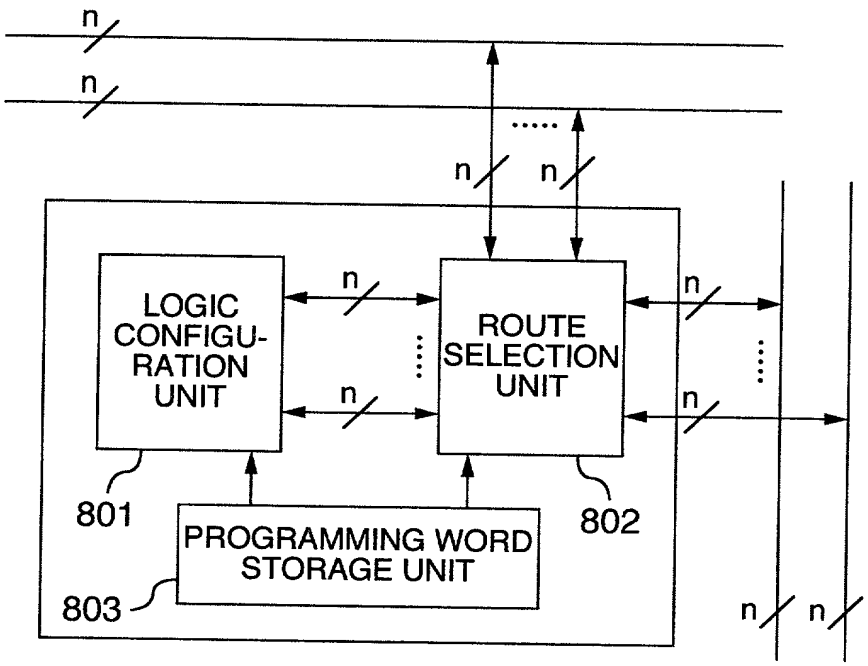
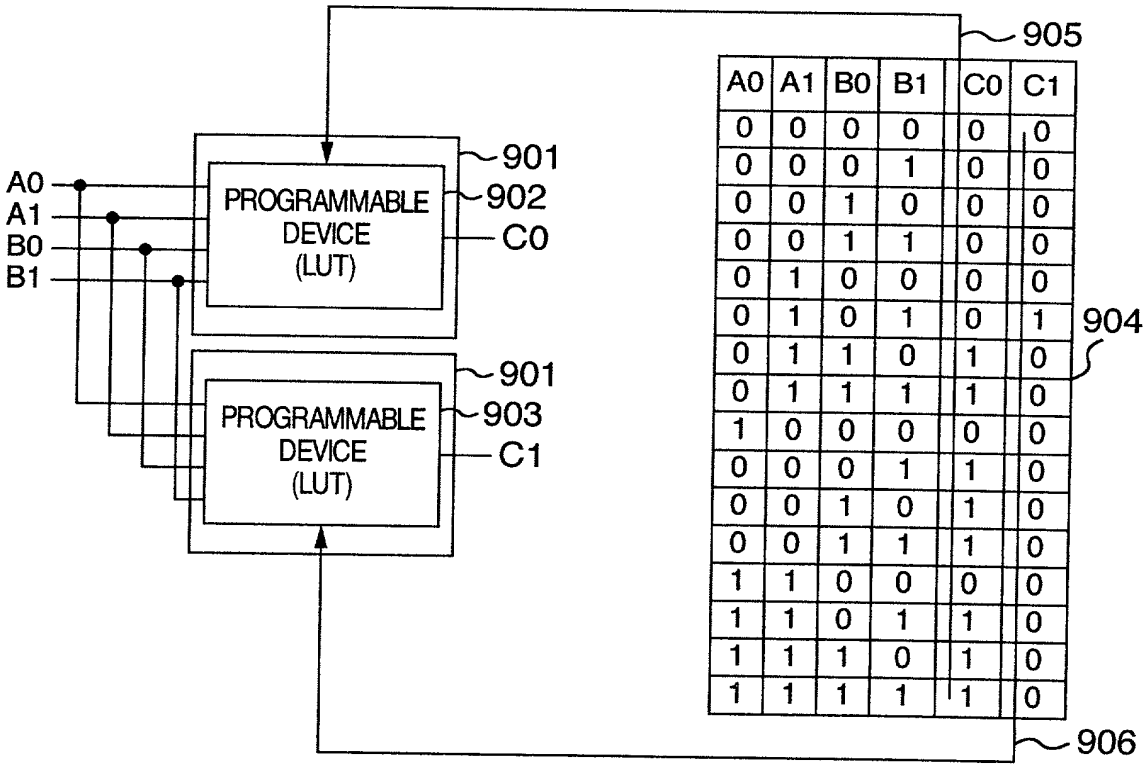
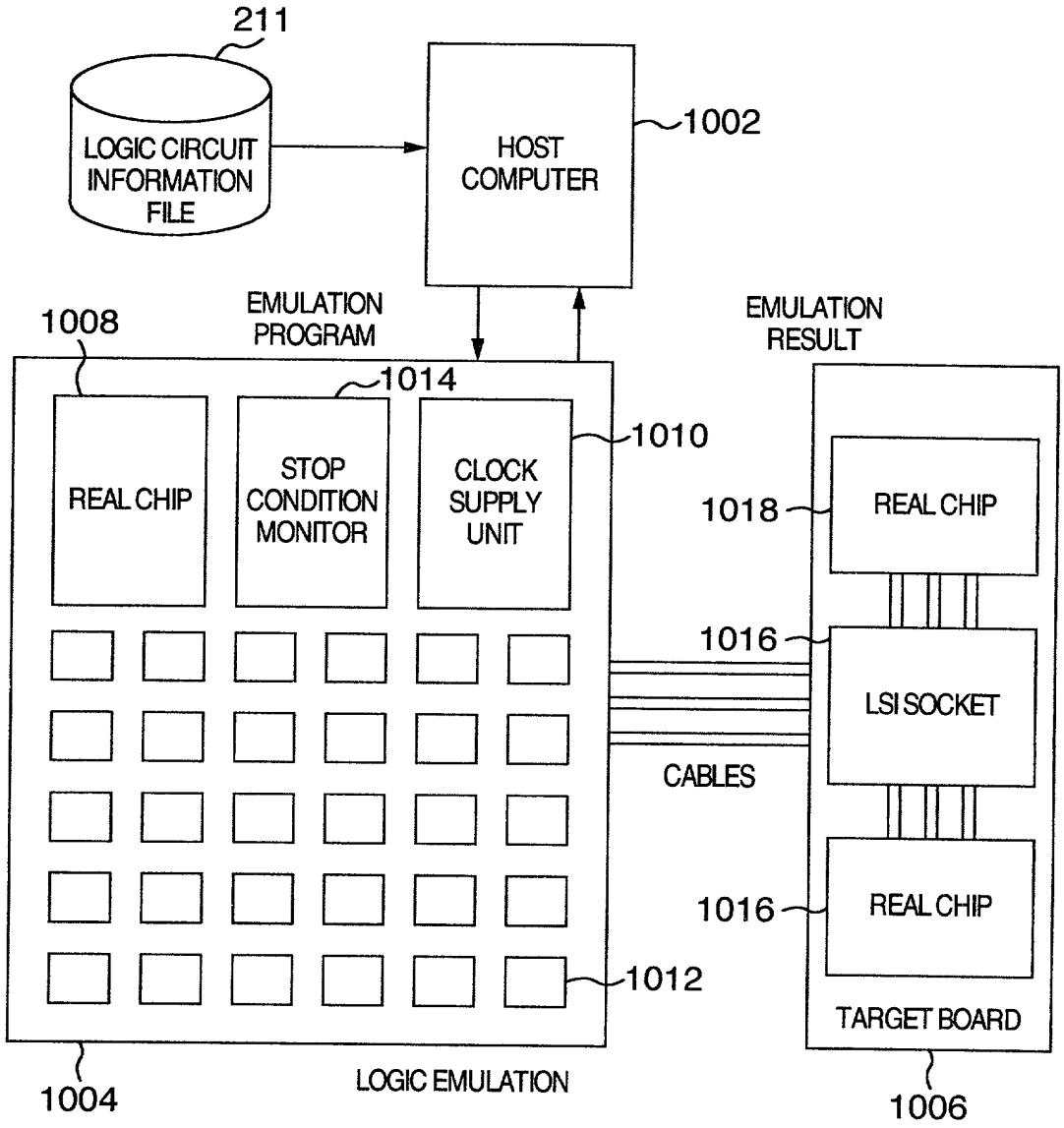


FIG. 9



A0	A1	B0	B1	C0	C1
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	1	0
1	1	0	0	0	0
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	1	0

FIG. 10


211
LOGIC CIRCUIT INFORMATION FILE
HOST COMPUTER
1002
EMULATION PROGRAM
EMULATION RESULT
1008
1014
REAL CHIP
STOP CONDITION MONITOR
CLOCK SUPPLY UNIT
1010
1018
REAL CHIP
1016
LSI SOCKET
CABLES
1016
REAL CHIP
1012
TARGET BOARD
1004
LOGIC EMULATION
1006